Claims 13-14 and 23 have been amended better to define the claimed invention.

Claims 1-27 stand rejected under 35 U.S.C. 102(e) as being anticipated by Teraoka et al. (6,097,113). Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of any of Claims 1-33 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." Verdegall Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1, as amended, requires and positively recites, a semiconductor device, comprising: "a logic circuit, which includes a MOS transistor" and "a bias voltage supply circuit, **comprising no more than two transistors**, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the MOS transistor".

In contrast, Teraoka discloses that voltage generation circuit 2a (that outputs bias supply voltage VP1 – the voltage higher than VDD) requires three transistors (2ac, 2ad, 2ae)(see figure 9). Teraoka further discloses that voltage generation circuit 2b (that outputs bias supply voltage VP2 – the voltage lower than VDD) requires three transistors (2ba, 2bf, 2bh)(see figure 6). Accordingly, Teraoka requires six transistors (and additional components) to accomplish what Applicants' circuitry does with no more than two transistors. As a result, Teraoka fails to teach or suggest, "a bias voltage supply circuit, **comprising no more than two transistors**, which selectively supplies a first bias voltage or a second bias voltage which

are different from each other to the substrate region of the MOS transistor", as required by Claim 1. The 35 U.S.C. 102(e) rejection is overcome.

Claims 2-7 stand allowable as depending, directly or indirectly, from allowable Claim 1 and including further limitations not taught or suggested by the references of record.

Claim 2 further defines the semiconductor device of Claim 1, wherein the bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 1.

Claim 3 further defines the semiconductor device of Claim 2, wherein the MOS transistor of the logic circuit is connected to the first voltage supply line. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 2.

Claim 4 further defines the semiconductor device of Claim 3, wherein the MOS transistor of the logic circuit and the first MOS transistor and second MOS transistor are PMOS transistors. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 3.

Claim 5 further defines the semiconductor device of Claim 4, wherein the logic circuit includes an NMOS transistor connected between the PMOS transistor and a third voltage supply line. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 4.

Claim 6 further defines the semiconductor device of Claim 1, wherein the first bias voltage is lower than the second bias voltage. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 1.

Claim 7 further defines the semiconductor device of Claim 1, further including at least one additional logic circuit coupled to the bias voltage supply circuit. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 1.

Independent Claim 8, as amended, requires and positively recites, a semiconductor device, comprising: "a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, a substrate region of said second MOS transistor **being permanently coupled to ground potential**" and "a bias voltage supply circuit which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor".

In contrast, Teraoka discloses that the substrate region of transistor N1 is selectively coupled to either VN1, GND or VN2 (see figure 1). As a result, Teraoka fails to teach or suggest, "a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, a substrate region of said second MOS transistor **being permanently coupled to ground potential**", as required by Claim 8. The 35 U.S.C. 102(e) rejection is overcome.

Claims 9-16 stand allowable as depending, directly or indirectly, from allowable Claim 8 and including further limitations not taught or suggested by the references of record.

Claim 9 further defines the semiconductor device of Claim 8, wherein the first MOS transistor is a PMOS transistor and the second MOS transistor is an NMOS transistor. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 8.

Claim 10 further defines the semiconductor circuit of Claim 8, wherein the first bias voltage is lower than the second bias voltage. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 8.

Claim 11 further defines the semiconductor circuit of Claim 8, wherein the first MOS transistor has a lower threshold voltage than said second MOS transistor. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 8.

Claim 12, as amended, further defines the semiconductor circuit of Claim 8, wherein the first bias voltage is lower than the supply line voltage. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 8.

Claim 13, as amended, further defines the semiconductor circuit of Claim 8, wherein the bias voltage supply circuit includes a third MOS transistor connected between a first voltage supply line and a bias voltage supply line and a fourth MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 8.

Claim 14, as amended, further defines the semiconductor circuit of Claim 13, wherein the first MOS transistor of the logic circuit is connected to the first voltage supply line. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 13.

Claim 15, as amended, further defines the semiconductor circuit of Claim 14, wherein the first MOS transistor of the logic circuit and the third MOS transistor and fourth MOS transistor are PMOS transistors. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 14.

Claim 16 further defines the semiconductor circuit of Claim 15, wherein the logic circuit includes an NMOS transistor connected between the PMOS transistor and a third voltage supply line. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 15.

Independent Claim 17, as amended, requires and positively recites, a semiconductor device, comprising: "a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential", "**a first bias voltage supply circuit, comprising no more than two transistors**, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor" and "**a second bias voltage supply circuit, comprising no more than two transistors**, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the second MOS transistor".

In contrast, Teraoka discloses that voltage generation circuit 2a (that outputs bias supply voltage VP1 – the voltage higher than VDD) requires three transistors (2ac, 2ad, 2ae)(see figure 9). Teraoka further discloses that voltage generation circuit 2b (that outputs bias supply voltage VP2 – the voltage lower than VDD) requires three transistors (2ba, 2bf, 2bh)(see figure 6). Accordingly, Teraoka requires six transistors (and additional components) to accomplish what Applicants' first bias voltage supply circuitry does with no more than two transistors. As a result, Teraoka fails to teach or suggest, "a first bias voltage supply circuit, **comprising no more than two transistors**, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor", as required by Claim 17.

Teraoka similarly discloses that voltage generation circuit 4a (that outputs bias supply voltage VN1 – a negative voltage lower than ground voltage (col. 6, lines 53-55)) requires three transistors (4ac, 4ad, 4ae)(see figure 8). Teraoka further discloses that voltage generation circuit 4b (that outputs bias supply voltage VN2 – a positive voltage higher than ground voltage GND (col. 6, lines 56-59)) requires three transistors (4bc, 4bd, 4be)(see figure 7). Accordingly, Teraoka requires six transistors (and additional components) to accomplish what Applicants' second bias voltage supply circuitry does with no more than two transistors. As a result, Teraoka fails to teach or suggest, "**a second bias voltage supply circuit, comprising no more than two transistors**, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the second MOS transistor", as required by Claim 17. The 35 U.S.C. 102(e) rejection is overcome.

Claims 18-27 stand allowable as depending, directly or indirectly, from allowable Claim 17 and including further limitations not taught or suggested by the references of record.

Claim 18 further defines the semiconductor device of Claim 17, wherein the first MOS transistor is a PMOS transistor and the second MOS transistor is an NMOS transistor. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 17.

Claim 19 further defines the semiconductor circuit of Claim 17, wherein the first bias voltage from the first bias supply circuit is lower than the second bias voltage from the first bias supply circuit. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 17.

Claim 20 further defines the semiconductor circuit of Claim 17, wherein the first bias voltage from the second bias supply circuit is lower than the second bias voltage from the second bias supply circuit. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 17.

Claim 21 further defines the semiconductor circuit of Claim 17, wherein the first MOS transistor has a lower threshold voltage than said second MOS transistor. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 17.

Claim 22 further defines the semiconductor circuit of Claim 17, wherein the first bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 17.

Claim 23, as amended, further defines the semiconductor circuit of Claim 17, wherein the second bias voltage supply circuit includes a third MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and ground potential and a second MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and a first bias supply line. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 17.

Claim 24 further defines the semiconductor circuit of Claim 17, wherein: "the first bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor" and "the second bias voltage supply circuit includes a third MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and ground potential and a fourth MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and a third bias supply line". The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 17.

Claim 25 further defines the semiconductor circuit of Claim 22, wherein the first and second MOS transistors of the first bias voltage supply circuit are PMOS transistors. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 22.

Claim 26 further defines the semiconductor circuit of Claim 23, wherein the first and second MOS transistors of the second bias voltage supply circuit are NMOS transistors. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 23.

Claim 27 further defines the semiconductor circuit of Claim 22, wherein the first and second MOS transistors of the first bias voltage supply circuit are PMOS transistors and the first and second MOS transistors of the second bias voltage supply circuit are NMOS transistors. The Teraoka reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 22.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Claims 1-27 stand allowable over the cited art and the application is in allowable form. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION – (marked-up version):

Please change the Title of the Invention from "Semiconductor Circuit" to --High Speed Semiconductor Circuit Having Low Power Consumption--.

Please delete the Abstract and replace with the following:

--A semiconductor circuit which can restrain increase in manufacturing cost and layout area to a minimum level and can realize high speed and low power consumption. Bias voltages with different levels are generated corresponding to a mode control signal by a bias voltage supply circuit comprising PMOS transistors P2 and P3 which have different voltages applied to the respective sources and the mode control signal input to the [respective] gates. The generated bias voltages are supplied to the n-wells of PMOS transistors. During operation, a bias voltage that is almost the same as the operation voltage is applied to the n-wells of PMOS transistors. During standby, a bias voltage higher than the operation voltage is supplied to the aforementioned n-wells of PMOS transistors. In this way, the driving currents of the transistors can be kept at a high level during operation, while leakage currents of the transistors can be restrained during standby. Consequently, high speed and low power consumption can be realized.--

IN THE CLAIMS – (marked-up version):

1. (amended) A semiconductor device, comprising:

a logic circuit, which includes a MOS transistor, and

a bias voltage supply circuit, comprising no more than two transistors, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the MOS transistor.

8. (amended) A semiconductor device, comprising:

a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, a substrate region of said second MOS transistor being permanently coupled to ground potential; and

a bias voltage supply circuit which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor.

12. (amended) The semiconductor circuit of Claim 8, wherein the first bias voltage is lower than the [second bias] supply line voltage.

13. (amended) The semiconductor circuit of Claim 8, wherein the bias voltage supply circuit includes a [first] third MOS transistor connected between a first voltage supply line and a bias voltage supply line and a [second] fourth MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor.

14. (amended) The semiconductor circuit of Claim 13, wherein the first MOS transistor of the logic circuit is connected to the first voltage supply line.

15. (amended) The semiconductor circuit of Claim 14, wherein the first MOS transistor of the logic circuit and the [first] third MOS transistor and [second] fourth MOS transistor are PMOS transistors.

17. (amended) A semiconductor device, comprising:

a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential;

a first bias voltage supply circuit, comprising no more than two transistors, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor; and

a second bias voltage supply circuit, comprising no more than two transistors, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the second MOS transistor.

23. (amended) The semiconductor circuit of Claim 17, wherein the second bias voltage supply circuit includes a [first] third MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and ground potential and a second MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and a first bias supply line.